SODIMM 4GB 1600MHZ

4GB 512M x 64-Bit 1Rank PC3L-12800

DESCRIPTION:

This document describes Kimtigo's 512M x 8-bit 1Rank 4GB DDR3L-1600 CL11 DRAM memory module, based on 8C 512M x8-bit DDR3L FBGA components.The SPD is programmed to JEDEC standard latency 1600Mhz timing of 11-11-11-28 at 1.35V. This 204-pin DIMM uses gold contact fingers and requires +1.35V. The electrical and mechanical specifications are as follows:

Features

DDR3L functionality and operations supported as Defined in the component data sheet

204Pin,small outline dual in-line memory module (SODIMM)

Fast data transfer rates:PC3-12800

VDD=1.35V + 0.100 / - 0.067V

Backward compatible to VDD=+1.5V ±0.075V

VDDSPD=+3.0V to +3.6V

Nominal and Dynamic On-die Termination(ODT) for data strobe and mask signals

On-board IC temperature sensor with integrated Serial Presence-Detect(SPD) EEPROM

Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the Mode Register Set (MRS)

Selectable BC4 or BL8 on-the fly (OTF)

Gold edge contacts

Halogen-free

Fly-by topology

Terminated control,command,and address bus

Operating temperature - Commercial (0℃≤TA≤+85℃)

Addressing

Parameter	512Meg x 8
Configuration	64Meg x 8bit x 8 banks
Refresh count	8K
ROW address	64K (A[15:0])
Bank address	8(BA[2:0])
Column address	1K (A[9:0])
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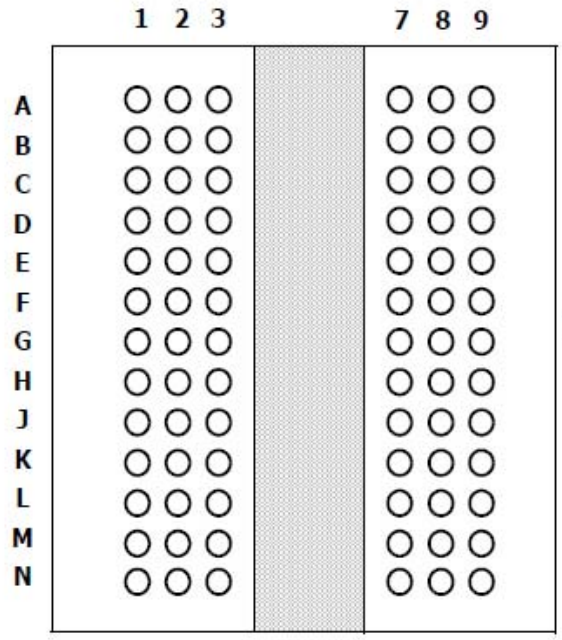
ordering Information

Memory Type	Density	Organization	Component Composition	#of ranks
Kimtigo DDR3 4GB 1R 1600MHZ	4GB	512M x 64bit	512X8 *8C	1

Kimtigo

x8 Package Ball out (Top view): 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VSS	VDD	NC				NF/$\overline{TDQS}$	VSS	VDD	A
B	VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ	B
C	VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	C
D	VSSQ	DQ6	$\overline{DQS}$				VDD	VSS	VSSQ	D
E	VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ	E
F	NC	VSS	$\overline{RAS}$				CK	VSS	NC	F
G	ODT	VDD	$\overline{CAS}$				$\overline{CK}$	VDD	CKE	G
H	NC	$\overline{CS}$	$\overline{WE}$				A10/AP	ZQ	NC	H
J	VSS	BA0	BA2				A15	VREFCA	VSS	J
K	VDD	A3	A0				A12/$\overline{BC}$	BA1	VDD	K
L	VSS	A5	A2				A1	A4	VSS	L
M	VDD	A7	A9				A11	A6	VDD	M
N	VSS	$\overline{RESET}$	A13				A14	A8	VSS	N
	1	2	3	4	5	6	7	8	9	

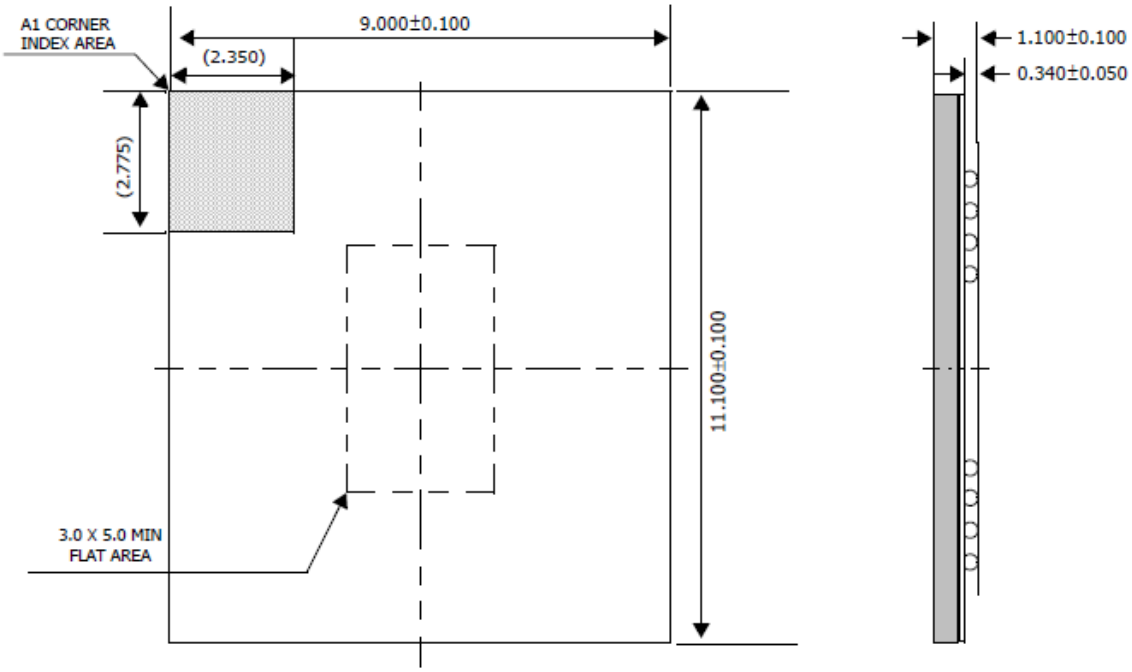


(Top View: See the balls through the Package)

○ Populated ball
+ Ball not populated

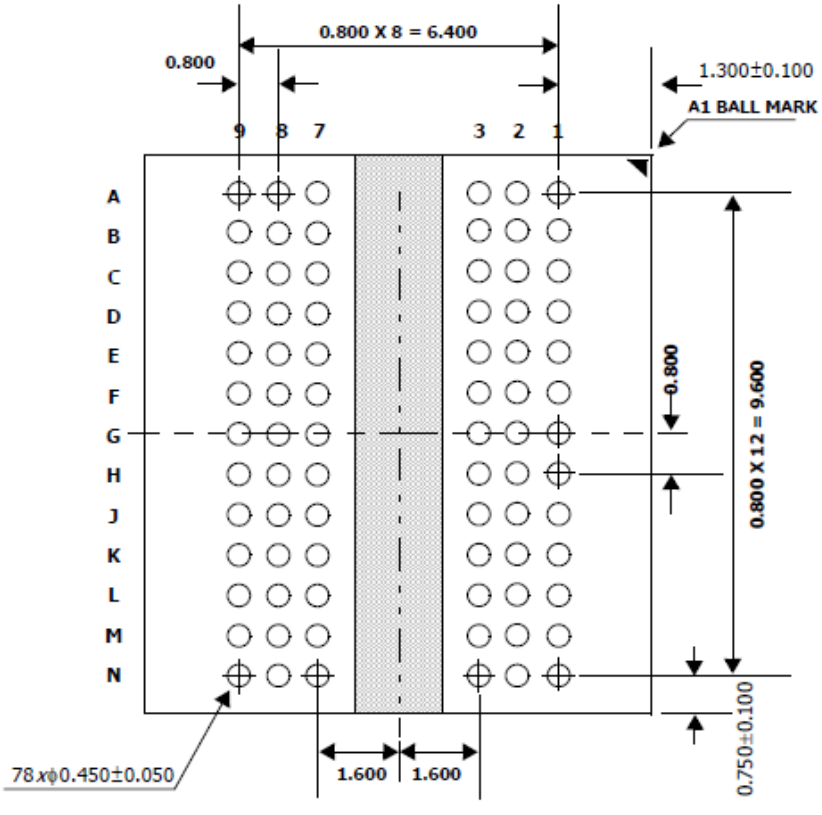
Package Dimensions

Package Dimension(x8): 78Ball Fine Pitch Ball Grid Array Outline



TOP VIEW

SIDE VIEW



BOTTOM VIEW

Pin Assignments

204-Pin DDR3 SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	53	DQ19	105	V_{DD}	157	DQ42
3	V_{SS}	55	V_{SS}	107	A10	159	DQ43
5	DQ0	57	DQ24	109	BA0	161	V_{SS}
7	DQ1	59	DQ25	111	V_{DD}	163	DQ48
9	V_{SS}	61	V_{SS}	113	WE#	165	DQ49
11	DM0	63	DM3	115	CAS#	167	V_{SS}
13	V_{SS}	65	V_{SS}	117	V_{DD}	169	DQS6#
15	DQ2	67	DQ26	119	A13	171	DQS6
17	DQ3	69	DQ27	121	S1#	173	V_{SS}
19	V_{SS}	71	V_{SS}	123	V_{DD}	175	DQ50
21	DQ8	73	CKE0	125	NC	177	DQ51
23	DQ9	75	V_{DD}	127	V_{SS}	179	V_{SS}
25	V_{SS}	77	NC	129	DQ32	181	DQ56
27	DQS1#	79	BA2	131	DQ33	183	DQ57
29	DQS1	81	V_{DD}	133	V_{SS}	185	V_{SS}
31	V_{SS}	83	A12	135	DQS4#	187	DM7
33	DQ10	85	A9	137	DQS4	189	V_{SS}
35	DQ11	87	V_{DD}	139	V_{SS}	191	DQ58
37	V_{SS}	89	A8	141	DQ34	193	DQ59
39	DQ16	91	A5	143	DQ35	195	V_{SS}
41	DQ17	93	V_{DD}	145	V_{SS}	197	SA0
43	V_{SS}	95	A3	147	DQ40	199	V_{DDSPD}
45	DQS2#	97	A1	149	DQ41	201	SA1
47	DQS2	99	V_{DD}	151	V_{SS}	203	V_{TT}
49	V_{SS}	101	CK0	153	DM5	–	–
51	DQ18	103	CK0#	155	V_{SS}	–	–

204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	V_{SS}	54	V_{SS}	106	V_{DD}	158	DQ46
4	DQ4	56	DQ28	108	BA1	160	DQ47
6	DQ5	58	DQ29	110	RAS#	162	V_{SS}
8	V_{SS}	60	V_{SS}	112	V_{DD}	164	DQ52
10	DQS0#	62	DQS3#	114	S0#	166	DQ53
12	DQS0	64	DQS3	116	ODT0	168	V_{SS}
14	V_{SS}	66	V_{SS}	118	V_{DD}	170	DM6
16	DQ6	68	DQ30	120	ODT1	172	V_{SS}
18	DQ7	70	DQ31	122	NC	174	DQ54
20	V_{SS}	72	V_{SS}	124	V_{DD}	176	DQ55
22	DQ12	74	CKE1	126	V_{REFCA}	178	V_{SS}
24	DQ13	76	V_{DD}	128	V_{SS}	180	DQ60
26	V_{SS}	78	NC/A15[1]	130	DQ36	182	DQ61
28	DM1	80	NC/A14[2]	132	DQ37	184	V_{SS}
30	RESET#	82	V_{DD}	134	V_{SS}	186	DQS7#
32	V_{SS}	84	A11	136	DM4	188	DQS7
34	DQ14	86	A7	138	V_{SS}	190	V_{SS}
36	DQ15	88	V_{DD}	140	DQ38	192	DQ62
38	V_{SS}	90	A6	142	DQ39	194	DQ63
40	DQ20	92	A4	144	V_{SS}	196	V_{SS}
42	DQ21	94	V_{DD}	146	DQ44	198	NF
44	V_{SS}	96	A2	148	DQ45	200	SDA
46	DM2	98	A0	150	V_{SS}	202	SCL
48	V_{SS}	100	V_{DD}	152	DQS5#	204	V_{TT}
50	DQ22	102	CK1	154	DQS5	–	–
52	DQ23	104	CK1#	156	V_{SS}	–	–

Notes: 1. Pin 78 is NC for 2GB and 4GB, A15 for 8GB.
2. Pin 80 is NC for 2GB, A14 for 4GB and 8GB.

Pin Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$, ($\overline{CS0}$), ($\overline{CS1}$), ($\overline{CS2}$), ($\overline{CS3}$)	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations.
$\overline{RAS}$. $\overline{CAS}$. $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/$\overline{TDQS}$ is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	Burst Chop: A12 / $\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.

Symbol	Type	Function
$\overline{RESET}$	Input	Active Low Asynchronous Reset: Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of V_{DD}, i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, $\overline{DQS}$, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS, DQSL, and DQSU are paired with differential signals $\overline{DQS}$, $\overline{DQSL}$, and $\overline{DQSU}$, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, $\overline{TDQS}$	Output	Termination Data Strobe: TDQS/$\overline{TDQS}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and $\overline{TDQS}$ is not used. x4 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
NF		No Function
V_{DDQ}	Supply	DQ Power Supply: 1.35 V +0.100/- 0.067 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.35 V +0.100/- 0.067 V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

Note:
Input only pins (BA0-BA2, A0-A15, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT, DM, and $\overline{RESET}$) do not supply termination.

B83SRCF 1.10 F3 1st DQ Map

Description: DDRIII SDRAM, Double-Ranks, x8-FBGA 78-based, x64, 204-pin Unbufferd SODIMM 1.0

Module Pin No.	Module DQ	Damping RES.	IC No.	IC DQ	Module Pin No.	Module DQ	Damping RES.	IC No.	IC DQ
5	0	RN30.6-RN30.3	U1	3	21	8	RN31.7-RN31.2	U7	2
7	1	RN30.7-RN30.2		7	23	9	RN31.8-RN31.1		4
15	2	RN31.5-RN31.4		0	33	10	RN32.7-RN32.2		1
17	3	RN31.6-RN31.3		2	35	11	RN32.8-RN32.1		3
4	4	RN42.8-RN42.1		5	22	12	RN43.6-RN43.3		6
6	5	RN42.7-RN42.2		1	24	13	RN43.5-RN43.4		0
16	6	RN43.8-RN43.1		4	34	14	RN44.6-RN44.3		7
18	7	RN43.7-RN43.2		6	36	15	RN44.5-RN44.4		5
39	16	RN33.5-RN33.4	U2	3	57	24	RN34.7-RN34.2	U19	2
41	17	RN33.6-RN33.3		7	59	25	RN34.8-RN34.1		4
51	18	RN34.5-RN34.4		0	67	26	RN35.6-RN35.3		1
53	19	RN34.6-RN34.3		2	69	27	RN35.8-RN35.1		3
40	20	RN45.8-RN45.1		5	56	28	RN46.5-RN46.3		6
42	21	RN45.7-RN45.2		1	58	29	RN46.6-RN46.4		0
50	22	RN46.8-RN46.1		4	68	30	RN47.6-RN47.3		7
52	23	RN46.7-RN46.2		6	70	31	RN47.5-RN47.4		5
129	32	RN36.6-RN36.3	U9	3	147	40	RN37.7-RN37.2	U12	2
131	33	RN36.5-RN36.4		7	149	41	RN37.8-RN37.1		4
141	34	RN37.5-RN37.4		0	157	42	RN38.6-RN38.3		1
143	35	RN37.6-RN37.3		2	159	43	RN38.1-RN38.8		3
130	36	RN48.8-RN48.1		5	146	44	RN49.6-RN49.3		6
132	37	RN48.6-RN48.3		1	148	45	RN49.5-RN49.4		0
140	38	RN49.8-RN49.1		4	158	46	RN50.6-RN50.3		7
142	39	RN49.7-RN49.2		6	160	47	RN50.5-RN50.4		5
163	48	RN39.5-RN39.4	U17	3	181	56	RN40.7-RN40.2	U11	2
165	49	RN39.6-RN39.3		7	183	57	RN40.8-RN40.1		4
175	50	RN40.5-RN40.4		0	191	58	RN41.7-RN41.2		1
177	51	RN40.6-RN40.3		2	193	59	RN41.8-RN41.1		3
164	52	RN51.8-RN51.1		5	180	60	RN52.6-RN52.3		6
166	53	RN51.7-RN51.2		1	182	61	RN52.5-RN52.4		0
174	54	RN52.8-RN52.1		4	192	62	RN53.6-RN53.3		7
176	55	RN52.7-RN52.2		6	194	63	RN53.5-RN53.4		5

B83SRCF 1.10 F3 2nd DQ Map Description: DDRIII SDRAM, Double-Ranks, x8-FBGA 82-based, x64, 204-pin Unbufferd SODIMM 1.0									
Module Pin No.	Module DQ	damping RES.	IC No.	IC DQ	Module Pin No.	Module DQ	damping RES.	IC No.	IC DQ
5	0	RN30.6-RN30.3	U16	2	21	8	RN31.7-RN31.2	U20	3
7	1	RN30.7-RN30.2		4	23	9	RN31.8-RN31.1		7
15	2	RN31.5-RN31.4		1	33	10	RN32.7-RN32.2		0
17	3	RN31.6-RN31.3		3	35	11	RN32.8-RN32.1		2
4	4	RN42.8-RN42.1		6	22	12	RN43.6-RN43.3		5
6	5	RN42.7-RN42.2		0	24	13	RN43.5-RN43.4		1
16	6	RN43.8-RN43.1		7	34	14	RN44.6-RN44.3		4
18	7	RN43.7-RN43.2		5	36	15	RN44.5-RN44.4		6
39	16	RN33.5-RN33.4	U15	2	57	24	RN34.7-RN34.2	U8	3
41	17	RN33.6-RN33.3		4	59	25	RN34.8-RN34.1		7
51	18	RN34.5-RN34.4		1	67	26	RN35.6-RN35.3		0
53	19	RN34.6-RN34.3		3	69	27	RN35.8-RN35.1		2
40	20	RN45.8-RN45.1		6	56	28	RN46.5-RN46.3		5
42	21	RN45.7-RN45.2		0	58	29	RN46.6-RN46.4		1
50	22	RN46.8-RN46.1		7	68	30	RN47.6-RN47.3		4
52	23	RN46.7-RN46.2		5	70	31	RN47.5-RN47.4		6
129	32	RN36.6-RN36.3	U18	2	147	40	RN37.7-RN37.2	U5	3
131	33	RN36.5-RN36.4		4	149	41	RN37.8-RN37.1		7
141	34	RN37.5-RN37.4		1	157	42	RN38.6-RN38.3		0
143	35	RN37.6-RN37.3		3	159	43	RN38.1-RN38.8		2
130	36	RN48.8-RN48.1		6	146	44	RN49.6-RN49.3		5
132	37	RN48.6-RN48.3		0	148	45	RN49.5-RN49.4		1
140	38	RN49.8-RN49.1		7	158	46	RN50.6-RN50.3		4
142	39	RN49.7-RN49.2		5	160	47	RN50.5-RN50.4		6
163	48	RN39.5-RN39.4	U10	2	181	56	RN40.7-RN40.2	U6	3
165	49	RN39.6-RN39.3		4	183	57	RN40.8-RN40.1		7
175	50	RN40.5-RN40.4		1	191	58	RN41.7-RN41.2		0
177	51	RN40.6-RN40.3		3	193	59	RN41.8-RN41.1		2
164	52	RN51.8-RN51.1		6	180	60	RN52.6-RN52.3		5
166	53	RN51.7-RN51.2		0	182	61	RN52.5-RN52.4		1
174	54	RN52.8-RN52.1		7	192	62	RN53.6-RN53.3		4
176	55	RN52.7-RN52.2		5	194	63	RN53.5-RN53.4		6

other problem.

	Clock loading	Boot failure
2-RANK	C65, C130, RN21	SPD data, U13 or U14

PCB 参数

Feature overview

PCB Information:

* Board size: 2661 x 1181 mil.

* Thickness: 40 ±4 mil.

* Panel: 6 pieces PCB per panel.

* 8-layer board.

* Impedance: 40/45/55/60(Single-ended) Ohm ±10%, 68/88(differential) Ohm ±15%.

* Pin count: 204 PIN.

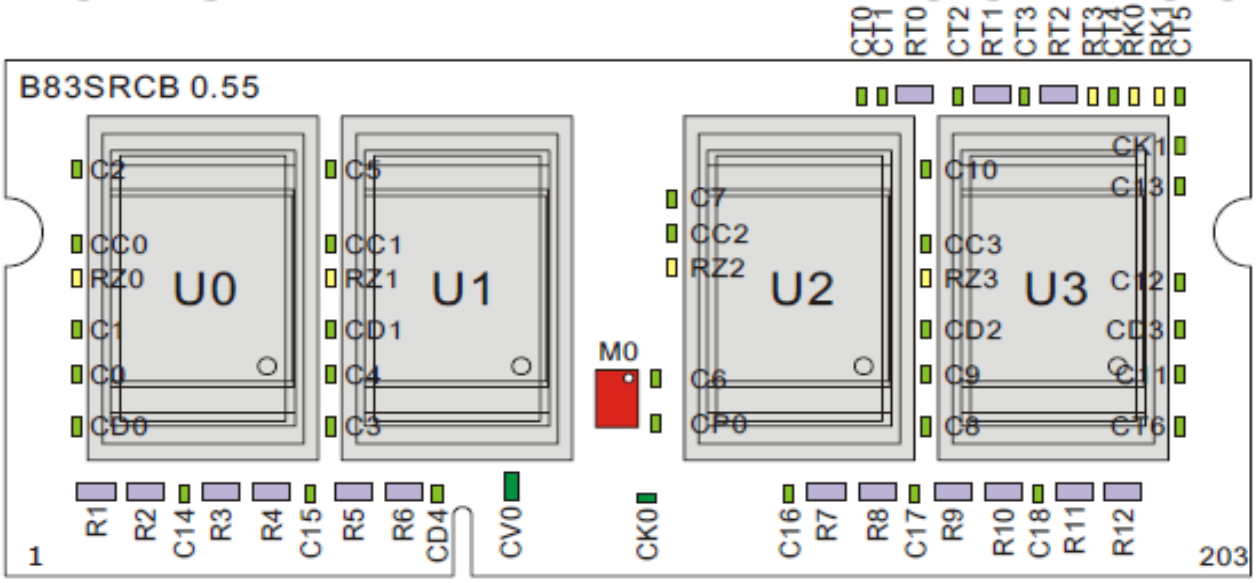
* 1.35~1.5V, 8K Refresh, FBGA, 78 Ball, 2Rank,8 banks DDRIII / L SDRAM based.

* Non-ECC DIMM organizations:

* 512MBx64 x1R

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TOP SIDE 1-RANK WITHOUT ECC



BOTTOM SIDE 1-RANK WITHOUT ECC

